Scaling and Biasing Analog Signals

November 2007

Introduction

Scaling and biasing the range and offset of analog signals is a useful skill for working with a variety of electronics. Not only can it interface equipment with different input and output voltage ranges together, it is also useful for designing circuits such as discrete transistor amplifiers. If you have a signal in one part of your circuit with a particular voltage range and offset, and need to map it to another range and offset, scaling and biasing will help. Several methods are presented here, including passive resistor designs and basic op amp techniques.

To begin, suppose you have an analog input signal $V_{in}(t)$, where V_{in} is a time dependent voltage. Scaling and biasing simply means computing a new signal $V_{out}(t)$:

$$V_{out}(t) \;=\; s \cdot V_{in}(t) \;+\; b \tag{1}$$

where the parameter s is called the *scale* and the parameter b the *bias*. The goal is to construct an analog electronic circuit that produces this linear transformation of V_{in} to V_{out}. Effectively, the circuit will be an analog computer for equation (1).

In elementary algebra, the parameters s and b are called the slope and offset of a straight line. The words *scale* and *bias* as used in electronics are synonyms for *slope* and *offset*. Setting aside for the moment that V_{in} and V_{out} depend on t, and focusing instead on V_{out} as a function of V_{in}, equation (1) is the graph of a straight line. In fact, given two (V_{in}, V_{out}) pairs on the straight line, we can compute s and b with:

$$s \;=\; \Delta V_{out}/\Delta V_{in} \tag{2}$$

$$b \;=\; V_{out} - s \cdot V_{in} \tag{3}$$

where either one of the (V_{in}, V_{out}) pairs can be used to compute b. The parameter s is dimensionless having the units $(volts/volts)$, while b has the dimensions of $volts$.

With these equations in hand, specifying the input and output ranges is equivalent to specifying s and b. For example, suppose you have a signal ranging from -100 to +100 volts, and you would like to map it into a (0,5) volt range. This is a common data acquisition problem where a sensor may not match an A/D input range. In this example, since we have $\Delta V_{in} = 200$ and $\Delta V_{out} = 5$, equation (2) gives:

$$s \;=\; \Delta V_{out}/\Delta V_{in} \;=\; 5/200 \;=\; 0.025$$

and with $V_{out} = 0$ when $V_{in} = -100$, equation (3) gives:

$$b \;=\; V_{out} - s \cdot V_{in} \;=\; 0 - s \cdot (-100) \;=\; 0.025 \cdot 100 \;=\; 2.5$$

so the final transformation between V_{out} and V_{in} for this case would be:

$$V_{out} \;=\; 0.025 \cdot V_{in} \;+\; 2.5$$

By testing various values in this equation you can verify it linearly maps voltages in the range of (-100,100) into (0,5) volts. Note that not only is the scale of the input voltage reduced by this particular transformation, negative inputs are mapped into a positive range as well.

Those familiar with oscilloscopes already know scaling and biasing. Scopes typically have one knob s to set the amplitude of the trace, and another knob b to translate it vertically up and down the display. Internally the scope has scaling and biasing circuits that can be set with the knobs.

This paper is about *designing* scaling and biasing circuits. *Given* s and b we would like to find a combination of resistors and other components to produce the transformation in equation (1). While not particularly difficult, the equations to compute component values are not trivial either. We will even find mathematical techniques such as projective transformations play an interesting role.

Two resistor circuits

Two resistor dividers are a convenient starting point for scaling and biasing. This section reviews the basic scaling divider, and then shows how to add a bias. We will find even though two resistor circuits have limitations regarding their bias, they are still useful for many applications. The next section, Three resistor circuits, will show how to implement designs which are even more flexible.

Consider the following two resistor scaling divider, where V_{in} is the input, V_{out} is the output, and (R_a, R_b) are the resistor values. Note that the labels V_{in} and V_{out} can be confusing because V_{in} is probably the *output* from some device on the left, *and* at the same time is the *input* to the divider. Don't confuse the meaning of the words *in* and *out* when working with the equations below. This paper assigns labels from the divider's point of view.

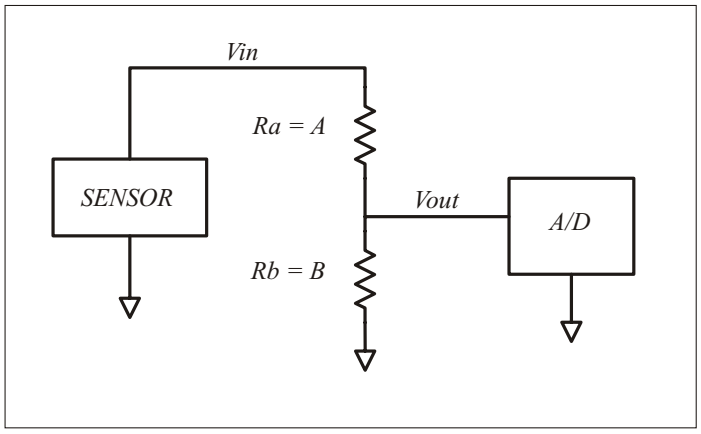

Figure 1: Basic two resistor scaling divider

Using Kirchoff's and Ohm's laws, and assuming no loading on V_{out}, the output voltage of this circuit is:

$$V_{out} \;=\; [\; R_b/(R_a + R_b)\;] \cdot V_{in} \tag{4}$$

The usual steps to derive this are: by Ohm's law, the *current* through the series combination (R_a, R_b) is: $V_{in}/(R_a + R_b)$. Then, since this is the same current flowing through R_b, the final output voltage is: $R_b \cdot [V_{in}/(R_a + R_b)]$. Deriving this equation should become automatic if you are working with these types of circuits. Equation (4) can also be derived formally by applying Kirchoff's and Ohm's laws to each node and leg of the circuit and solving the resulting simultaneous equations.

Note that equation (4) can be written as:

$$V_{out} = [\ (B/A)\ /\ (1 + (B/A))\ ] \cdot V_{in} \tag{5}$$

where two changes have been made. First, the resistor values have been denoted by capital letters, $A = R_a$ and $B = R_b$ to reduce the number of subscripts. We will follow that pattern in the rest of this this paper. Second, the top and bottom of equation (4) have been multiplied by $1/A$ to show *it is only the ratio* B/A that determines the output voltage. Sometimes, if B is much less than A, it may even be possible to approximate the output as $(B/A)V_{in}$, however here we will keep the equation exact so it is applicable to precision work.

The simple divider in Figure 1 is suitable for applications where only scaling is required. Note equation (4) or (5) is the same as equation (1) with $s = B/(A + B)$ and $b = 0$. That is to say it is a transformation with no bias or offset. As a specific example, suppose you have a sensor with an output range of 0 to 50 volts and wish to map that into a 0 to 5 volt range. Choosing $A = 90$K ohms and $B = 10$K would scale the input by $10/(10 + 90) = 0.10$, and the (0,50) volt sensor would be divided down to (0,5) volts. The circuit is:

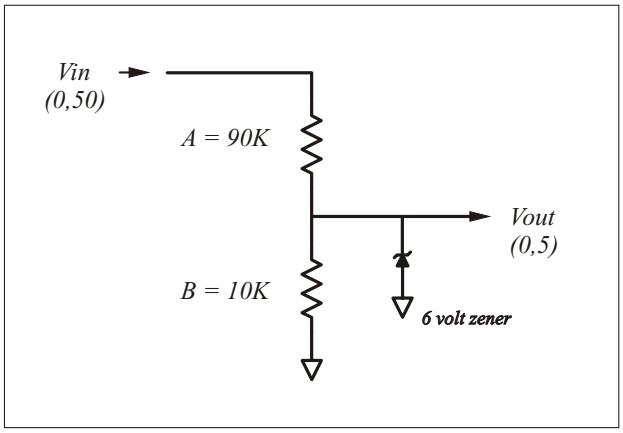

Figure 2: Scaling (0,50) into (0,5) with no bias

If you build this circuit, be careful the high input voltage is never accidentally connected directly to V_{out}, because you might damage any downstream equipment. A 6 volt zener across the output would be a reasonable first step towards protection.

Even though it is only the ratio B/A that determines the output in equation (4), also keep in mind that *there are currents* flowing in the resistors. With a 90K and 10K

pair, a maximum current of 50v/100K = 1/2 milliamp will flow in the divider. This is good, the resistors will not overheat, and hopefully the input source can provide that amount of current. *Do not* use a 9 ohm and 1 ohm resistor in Figure 2.

While the simple scaling divider is fine for applications requiring only scaling, it does not add any bias. Negative voltages going into the divider come out negative, while you may require such voltages to be biased into the positive range. This can be done by modifying the basic divider as shown in Figure 3. The circuit is the same as the simple scaling divider *except* the end of resistor B is held at a nonzero voltage and *not* at ground.

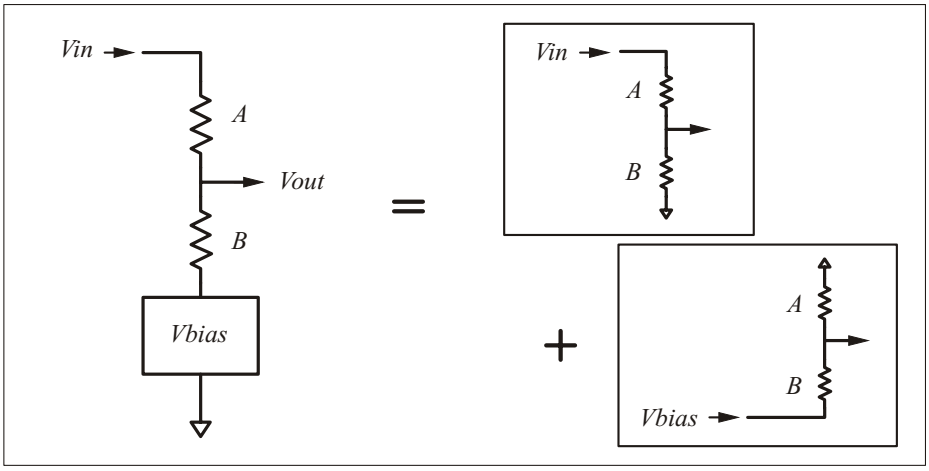

Figure 3: Biased two resistor divider

The output of the biased divider in Figure 3 is:

$$V_{out} \quad = \quad [B/(A+B)] \cdot V_{in} \quad + \quad [A/(A+B)] \cdot V_{bias} \tag{6}$$

With practice, equations like (6) can be written down at sight. Here is how: from Kirchoff's and Ohm's laws we know V_{out} must be a *linear homogeneous* function of V_{in} and V_{bias}. Because of that we can solve for V_{out} with V_{in} and V_{bias} alternately set to zero and then add the partial results together to form the complete answer. The partial results for V_{in} and V_{bias} are easy to write down because they are each the same as the simple scaling resistor divider without bias. This decomposition is indicated with the subdiagrams in Figure 3.

Comparing the biased divider equation (6) with equation (1), we can see it is a full linear transformation with scaling *and biasing* given by:

$$s = [\ B/(A+B)\ ] \tag{7}$$
$$b = [\ A/(A+B)\ ] \cdot V_{bias} \tag{8}$$

where b is now a nonzero value. Progress! We have a linear transformation including bias. Note the value of b is *not the same* as the V_{bias} bias voltage. The resistors A and B scale not only the input signal, but *also* the bias voltage. Because of this, the equations between (s, b) and (A, B, V_{bias}) are coupled. Despite this, a simple circuit for equation (1) results and is very useful.

As a forward example with equation (6), suppose we try $B = A$ and $V_{bias} = 5.0$, then:

$$V_{out} = V_{in}/2 + 2.5 \tag{9}$$

and an input range of (-5,+5) volts is mapped into (0,5). We have successfully mapped an input range including negative voltages into a purely positive range, and only required a single positive bias voltage to do it! The corresponding circuit is:

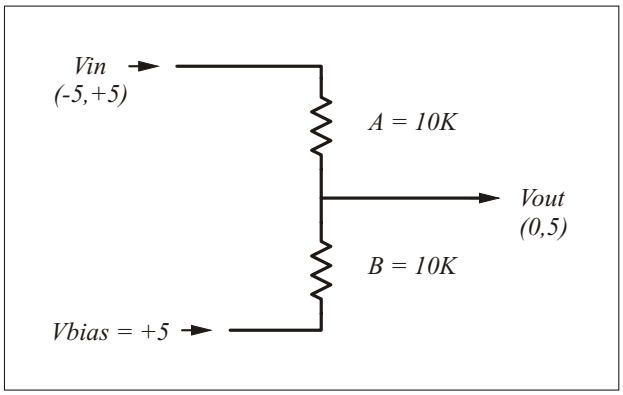

Figure 4: Scaling and biasing (-5,+5) into (0,5) with $V_{bias} = +5.0$

You can breadboard this in any convenient fashion and measure the input and output with a scope. A sine wave generator makes a good input signal for testing, and an adjustable lab power supply can provide the bias voltage. This simple circuit can be quite useful for interfacing various types of equipment together.

Of course, in actual practice the design goal is to go the other way with equation (6). *Given* the ranges for V_{in} and V_{out}, the problem is to *determine* the required values of

(A, B, V_{bias}). To do that, follow a two step design process. First start with the V_{in} and V_{out} ranges, and use equations (2) and (3) to determine s and b. Then use the value of s with equation (7) to determine the ratio $r = B/A$, followed by equation (8) to determine the required V_{bias}.

Combining the algebra into one set of equations arrives at:

$$r = \Delta V_{out} \ / \ (\Delta V_{in} - \Delta V_{out}) \quad (10)$$

$$V_{bias} = V_{out} - r \cdot (V_{in} - V_{out}) \quad (11)$$

where $r = B/A$, and (V_{in}, V_{out}) is any pair of input/output values. As usual, while any resistors with the ratio r will work, use values large enough to keep the divider currents small. Also note the value of V_{bias} is fixed by the design process. With these equations in hand, the design steps for a biased two resistor divider in Figure 3 are:

Step 1: Determine the required input and output ranges from spec sheets or experiment:

ΔV_{in} = divider input span (= sensor output range)

ΔV_{out} = divider output span (= A/D input range)

Step 2: Compute the resulting resistor ratio:

$$r = B/A = \Delta V_{out}/(\Delta V_{in} - \Delta V_{out})$$

Step 3: and, compute the required bias voltage:

$$V_{bias} = V_{out} - r \cdot (V_{in} - V_{out})$$

where the V_{in} and V_{out} in step 3 are any convenient pair of input and output voltages. Note that when working by hand, these computations are often best done as fractions which are easy to write down with no loss of precision.

Let's see if these design steps work with the above example that started with $B = A$ and $V_{bias} = 5.0$, but going in the reverse direction instead. Beginning with the input and output ranges, (-5,+5) and (0,5), we first compute $\Delta V_{in} = 10$ and $\Delta V_{out} = 5$. Then applying step 2 gives:

$$r = 5 \ / \ (10-5) = 1$$

or $B = A$, and computing step 3 with $V_{in} = -5.0$ mapping into $V_{out} = 0.0$ gives:

$$V_{bias} \;=\; 0 - 1(-5 - 0) \;=\; 5.0 \text{ volts}$$

all agreeing with the results we should get.

The table in Figure 5 computes the values of (A, B, V_{bias}) required to map a variety of bipolar input ranges into a (0,5) output, a popular range for A/D equipment. Note the (A, B) values have been scaled so A is always a 10K ohm resistor. You can scale to other values as appropriate, just keep the divider currents in the low milliamp range. Regardless of what scaled resistor values are used, V_{bias} must be as shown. The line marked with a $\star$ is the same as the circuit in Figure 4.

	Bipolar input	ΔV_{in}	V_{out}	A(Kohm)	B(Kohm)	V_{bias}
	(+/-) 03.0	6.0	(0,5)	10.000	50.000	15.00
	(+/-) 04.0	8.0	(0,5)	10.000	16.667	6.67
$\star$	(+/-) 05.0	10.0	(0,5)	10.000	10.000	5.00
	(+/-) 06.0	12.0	(0,5)	10.000	7.143	4.29
	(+/-) 07.0	14.0	(0,5)	10.000	5.556	3.89
	(+/-) 08.0	16.0	(0,5)	10.000	4.545	3.64
	(+/-) 09.0	18.0	(0,5)	10.000	3.846	3.46
	(+/-) 10.0	20.0	(0,5)	10.000	3.333	3.33
	(+/-) 11.0	22.0	(0,5)	10.000	2.941	3.24
	(+/-) 12.0	24.0	(0,5)	10.000	2.632	3.16
	(+/-) 13.0	26.0	(0,5)	10.000	2.381	3.10
	(+/-) 14.0	28.0	(0,5)	10.000	2.174	3.04
	(+/-) 15.0	30.0	(0,5)	10.000	2.000	3.00

Figure 5: (A, B, V_{bias}) values for mapping various input ranges into (0,5)

Note that the (A, B, V_{bias}) values in the table above are for input ranges balanced evenly around 0. In fact, the design steps work equally well for *unbalanced inputs*. Balanced input is only the most common case.

As an example of unbalanced input, consider mapping the input range of (-5,+10) into the range (0,5). Using the design steps, the calculation in Figure 6 results. To build a circuit for this example, choose any two resistors with the ratio 1/2. The values

B = 10K and A = 20K would be appropriate. If you don't have a 20K resistor on hand, build one from two 10K resistors in series. Use a lab power supply or op amp to generate the required 2.5 volt bias voltage and you are done.

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Unbalanced input design example:

                  Sensor range = (-5,+10)
                     A/D range = (0,5)

          -> Divider input span = 15 volts
         -> Divider output span = 5 volts

                             r = 5/(15-5) = 1/2  ( = B/A resistor ratio )
                        Vbias = 0 - 1/2 * (-5 - 0) = 2.5 volts
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Figure 6: Scaling and biasing an unbalanced (-5,+10) into (0,5) with $V_{bias} = +2.5$

When working with biased resistor dividers, V_{bias} must be *constant. This is crucial.* Any change in V_{bias} will become a variation or noise on V_{out}. You must have access to a bias voltage that is low impedance, well regulated, and noise free. Often such a voltage is available from an A/D reference voltage on the data acquisition equipment, or perhaps from a power supply.

Also note for two resistor circuits, the required bias voltages are a *result* of the design steps, and odd values of V_{bias} may be required. If you need to map (-6,+6) into (0,5) and don't have access to a bias voltage like 4.29 volts, the next section reviews *three* resistor circuits allowing the bias to be specified as part of the design. Do not use a resitive divider to generate odd bias voltages. The output from such a divider will not stay constant as V_{in} varies. It is easier to use the circuits discussed in the next section or op amp techniques.

Generally, scaling and biasing with resistor dividers achieves good results. Besides being simple, if metal film resistors with a low TC and a well regulated low impedance bias voltage are used, such circuits add little noise to a signal. Sometimes, the input impedance of a resistive divider may be a concern. However, for applications with active sensors, this is usually not a problem because such sensors typically have output amplifiers capable of driving resistor dividers. When input impedance is an issue consider the techniques in the op amp section.

Three resistor circuits

For the two resistor designs in the previous section, the required bias voltage is fixed by the input and output ranges, and may not be a convenient value. With the addition of one resistor, the bias voltage may be *specified* as part of the design process. Figure 7 shows the three resistor circuit, where the additional resistor C is connected from the V_{out} node to ground.

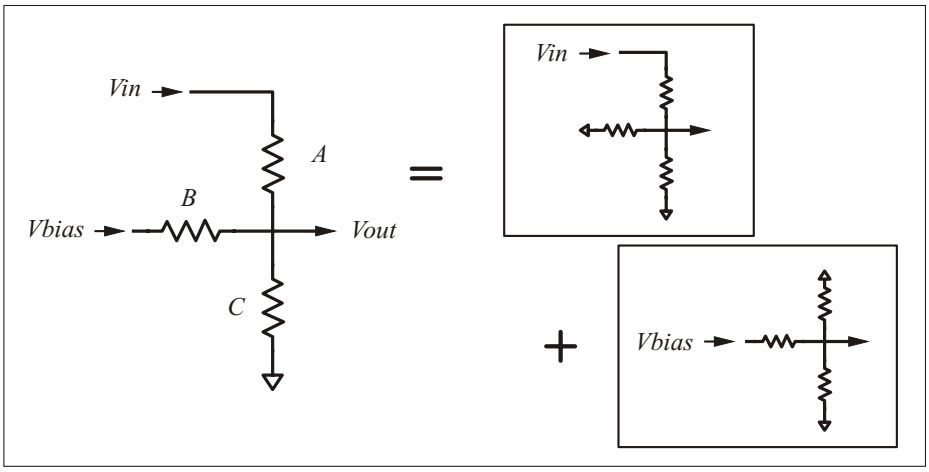

Figure 7: Biased three resistor divider

Using linearity and superposition of partial results, the output voltage for this circuit can be written down at sight as:

$$V_{out} \;=\; [\,(B|C)\;/\;(A+(B|C))\,]\cdot V_{in} \;\;+\;\; [\,(A|C)\;/\;(B+(A|C))\,]\cdot V_{bias} \qquad (12)$$

where | denotes the parallel combination of two resistors: $(B|C) = (B \cdot C)/(B + C)$. In equation (12) the additional degree of freedom C beyond the two resistor equation (6) allows for the value of V_{bias} to be *specified* rather than fixed by the design process. Comparing equation (12) with equation (1) we can see it is a full linear transformation with:

$$s \;=\; [\,(B|C)\;/\;(A+(B|C))\,] \qquad (13)$$

$$b \;=\; [\,(A|C)\;/\;(B+(A|C))\,]\cdot V_{bias} \qquad (14)$$

where our design goal is: given (s, b, V_{bias}) to compute (A, B, C). Clearly the relationship between (s, b) and the resistors is more complicated than the two resistor equations (7) and (8), and one might even wonder if it is nonlinear. Actually, things are simpler than they appear at first. To see this, start over with Kirchoff's and Ohm's law at the V_{out} node in Figure 7:

$$(V_{out} - V_{in})/A \ + \ (V_{out} - V_{bias})/B \ + \ V_{out}/C = 0 \tag{15}$$

Assuming no external loading at V_{out}, this equation specifies the sum of the currents is conserved. The current flowing into the node is matched by that flowing out. Of course with algebra equation (15) can be derived from equation (12), but starting from first principles is more direct. Sometimes this circuit is redrawn and referred to as a Y connection for three resistors as in Figure 8.

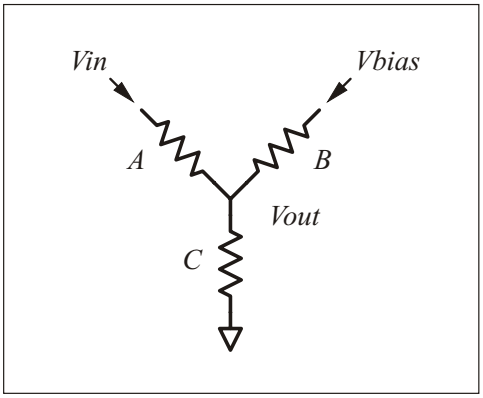

Figure 8: Y connection

Rearranging (15) into transfer equation form results in:

$$V_{out} \cdot (1/A + 1/B + 1/C) \ = \ V_{in}/A \ + \ V_{bias}/B \tag{16}$$

or

$$V_{out} \ = \ V_{in}/(A \cdot (1/A + 1/B + 1/C)) \ + \ V_{bias}/(B \cdot (1/A + 1/B + 1/C)) \tag{17}$$

Equation (15) is linear in the conductances $(1/A, 1/B, 1/C)$. We won't make much use of that fact here. However, these equations are also *homogeneous* in (A, B, C).

That is to say, multiplying (A, B, C) all by the same constant λ results in another set of resistors that solve the equations equally well. This mapping of one solution into another will be useful.

Comparing equation (17) with equation (1), we see the values for (s, b) are:

$$\begin{aligned} s &= (\ 1\ /\ [\ A \cdot (1/A + 1/B + 1/C)\ ]\ ) && (18) \\ b &= (\ 1\ /\ [\ B \cdot (1/A + 1/B + 1/C)\ ]\ ) \cdot V_{bias} && (19) \end{aligned}$$

These are of course the same as equations (13) and (14), just in different algebraic form. Given (s, b, V_{bias}), we'd like to solve these *two* equations for the *three* unknowns (A, B, C). At first it might seem as if there are fewer equations than unknowns in (18) and (19), and the system is under determined. But, multiplying the top and bottom of each equation by C, the pair can be rewritten as:

$$\begin{aligned} s &= (\ (C/A)\ /\ (C/A + C/B + 1)\ ) \\ b &= (\ (C/B)\ /\ (C/A + C/B + 1)\ ) \cdot V_{bias} \end{aligned}$$

to show there are really only two equations in the two unknown ratios (C/A) and (C/B), which could then be solved. Rather than solving these equations directly, here is an even easier way to proceed:

From equation (15) we know any multiple $\lambda(A, B, C) \equiv (A_\lambda, B_\lambda, C_\lambda)$ of a given solution is also solution. For a particularly convenient scaling, choose:

$$\lambda = (1/A + 1/B + 1/C)$$

and then the pair (18) and (19) becomes:

$$\begin{aligned} s &= 1/A_\lambda && (20) \\ b &= V_{bias}/B_\lambda && (21) \end{aligned}$$

This *decoupled* pair for (A_λ, B_λ) is easy to solve and combine with equations (2) and (3) for s and b in terms of the input and output voltage ranges giving:

$$\begin{aligned} A_\lambda &= \Delta V_{in}/\Delta V_{out} && (22) \\ B_\lambda &= V_{bias}/(V_{out} - V_{in}/A_\lambda) && (23) \\ C_\lambda &= 1/(1 - 1/A_\lambda - 1/B_\lambda) && (24) \end{aligned}$$

The last equation for C_λ reflects the scaling λ we have chosen. To see this start with:

$$1/A_\lambda + 1/B_\lambda + 1/C_\lambda \;=\; (1/\lambda)\cdot(1/A + 1/B + 1/C) \;=\; 1$$

and solve the left for C_λ in terms of (A_λ, B_λ), yielding equation (24). To summarize, the linear homogeneous symmetry of equation (15) has been used to find one particularly easy solution, and now other solutions can be obtained by simply scaling $(A_\lambda, B_\lambda, C_\lambda)$ as needed. This type of symmetry is known as a projective transformation. Such transformations have a long and fascinating history, often achieving surprising results as in the photo at the end of this paper.

With these equations in hand, the general design steps for the biased three resistor circuit in Figure 7 are:

Step 1: Determine the input and output ranges from spec sheets or experiment:

ΔV_{in} = divider input span (= sensor output range)

ΔV_{out} = divider output span (= A/D input range)

Step 2: Compute $(A_\lambda, B_\lambda, C_\lambda)$ from:

$A_\lambda = \Delta V_{in}/\Delta V_{out}$

$B_\lambda = V_{bias}/(V_{out} - V_{in}/A_\lambda)$

$C_\lambda = A_\lambda B_\lambda/(A_\lambda B_\lambda - A_\lambda - B_\lambda)$

where V_{out} and V_{in} in the B_λ equation are any convenient input and output pair. When computing by hand, it may be easiest to carry the calculation as fractions.

Step 3: Scale $(A_\lambda, B_\lambda, C_\lambda)$ to the desired values. For example, if A = 10K ohm is desired then compute:

$A = (10K/A_\lambda) * A_\lambda = 10K$

$B = (10K/A_\lambda) * B_\lambda$

$C = (10K/A_\lambda) * C_\lambda$

The table in Figure 9 gives the three resistor values (A, B, C) to map a variety of bipolar input ranges into the output range V_{out} = (0,5) using V_{bias} = 5.0 volts. These values should be used with the circuit in Figure 7. The resistor values have been scaled

so A is 10K ohms. Multiply (A, B, C) all by the same constant to scale to other values, where for safe divider currents, keep the resistors in the Kohm range. Of course the thing to note about this table is all the mappings use the same bias voltage, 5.0 volts in the last column. This should be compared with the two resistor table.

	Bipolar input	ΔV_{in}	V_{out}	A(Kohm)	B(Kohm)	C(Kohm)	V_{bias}
	(+/-) 05.0	10.0	(0,5)	10.000	10.000	******	5.00
	(+/-) 06.0	12.0	(0,5)	10.000	8.333	50.000	5.00
	(+/-) 07.0	14.0	(0,5)	10.000	7.143	25.000	5.00
	(+/-) 08.0	16.0	(0,5)	10.000	6.250	16.667	5.00
	(+/-) 09.0	18.0	(0,5)	10.000	5.556	12.500	5.00
⋆	(+/-) 10.0	20.0	(0,5)	10.000	5.000	10.000	5.00
	(+/-) 11.0	22.0	(0,5)	10.000	4.545	8.333	5.00
	(+/-) 12.0	24.0	(0,5)	10.000	4.167	7.143	5.00
	(+/-) 13.0	26.0	(0,5)	10.000	3.846	6.250	5.00
	(+/-) 14.0	28.0	(0,5)	10.000	3.571	5.556	5.00
	(+/-) 15.0	30.0	(0,5)	10.000	3.333	5.000	5.00
	(+/-) 16.0	32.0	(0,5)	10.000	3.125	4.545	5.00
	(+/-) 17.0	34.0	(0,5)	10.000	2.941	4.167	5.00
	(+/-) 18.0	36.0	(0,5)	10.000	2.778	3.846	5.00
	(+/-) 19.0	38.0	(0,5)	10.000	2.632	3.571	5.00
	(+/-) 20.0	40.0	(0,5)	10.000	2.500	3.333	5.00

Figure 9: Three resistor values for mapping various input ranges into (0,5)

The case of a (-10,+10) input range marked with a ⋆ in the table is of particular interest for many applications. The circuit for this is shown in the following figure. A/D references can provide the bias voltage, as well as power supplies in some cases. If you don't have a 5K resistor on hand, build it from two 10K resistors in parallel.

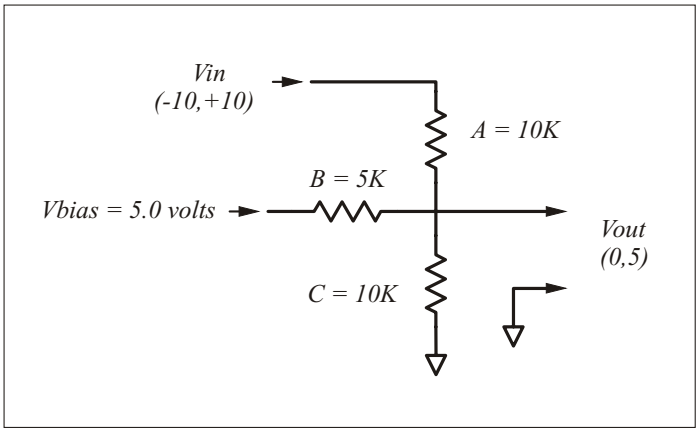

Figure 10: Three resistor scaling and biasing (-10,+10) into (0,5) with $V_{bias} = +5.0$

By comparison, a two resistor divider requiring a less convenient 3.3 volt bias is shown in the following figure. However, we will see in the next section even this is reasonably easy to use when combined with an op amp.

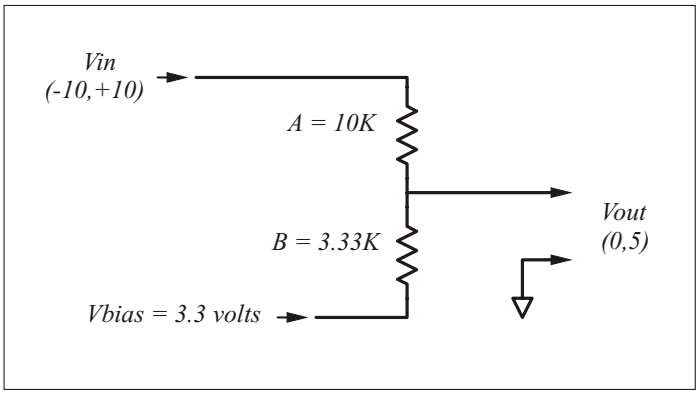

Figure 11: Two resistor scaling and biasing (-10,+10) into (0,5) with $V_{bias} = +3.3$

It is worth noting the projective transformations used in this section can be applied to more complicated networks with additional resistors, as well as the analysis of circuits involving *complex impedances* with sinusoidal AC voltages. Sometimes difficult phase relationships can be reduced to *decoupled equations* when scaled properly. The scaling factor λ may itself become complex, but the algebraic structure remains the same as with purely resistive elements.

Op Amp techniques

Adding op amps to scaling and biasing circuits provides possibilities beyond the passive resistor dividers already covered. For example, op amps can be used to increase the input impedance of a resistor divider, lower the output impedance of a resistor divider, add gain to signals, and perform other circuit functions. This section will review a few circuit examples, but does not give full design steps as in the previous sections.

A good feature of op amps is their naturally high input impedance. Passive resistor dividers have the input impedance of their resistors. For applications where a very high input impedance is required, an op amp can buffer a resistive divider input into the high Mohm range. However, keep in mind high input impedance can increase noise pickup on long input cables and consider working with lower input impedances if you anticipate noise problems. Besides buffering the input impedance, op amps can also drive significant loads and be used to lower the output impedance of passive resistor networks.

A bad feature of op amps is they require a power supply. Not only that, if the op amp must handle bipolar input signals, then a split +/- supply will be probably be required. Often something like +/-12 volts. Providing a split supply increases the complexity of implementing op amp circuits. For this discussion, we assume users are familiar with these issues and have their own preferred solutions. Power supply and ground connections are not shown in the circuit fragments reviewed here but are essential for proper operation.

Circuits involving op amps can be as simple as unity gain buffers:

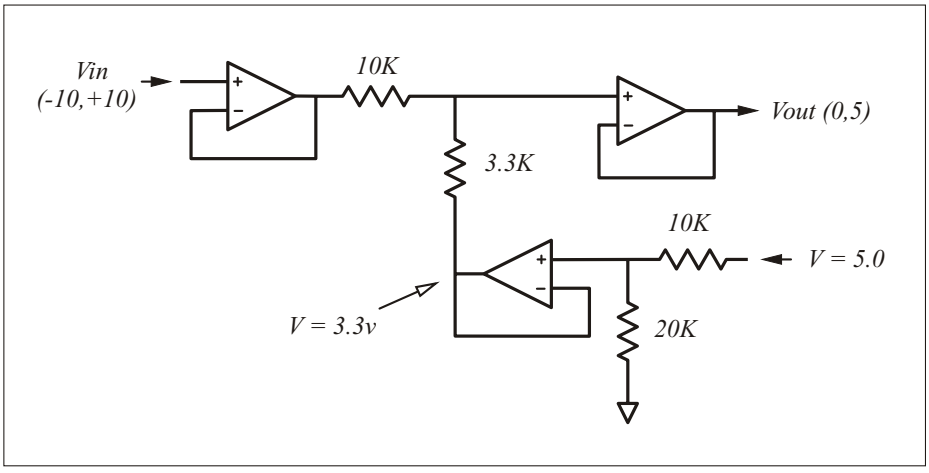

Figure 12: Op amp unity gain buffer with scaling

This circuit buffers a (-10,+10) signal with a unity gain amplifier on the left to provide high input impedance. The output of the input buffer is then scaled and biased with a two resistor divider. For +/-10 input to be scaled to (0,5) output, the two resistor divider requires a 3.3 volt bias, as listed in the two resistor table in Figure 5. Here, the bias is formed from a 5 volt reference and a resistor divider which is then buffered with its own unity gain amplifier so the 3.3 volts has low output impedance and will not vary. Finally, the signal output is also buffered for a low output impedance. When implementing this circuit, you will have to provide power for the op amps. For the resistors, you can build a 3.3K resistor from three 10K resistors in parallel. Although simple, this circuit is capable of good performance.

The circuit in Figure 13 makes further modifications to give the front end a gain of 10. With this configuration, the full scale input range becomes (+/-500mV). Here, for scaling and biasing after the gain stage, a two resistor divider is used with 5 volts as the bias source.

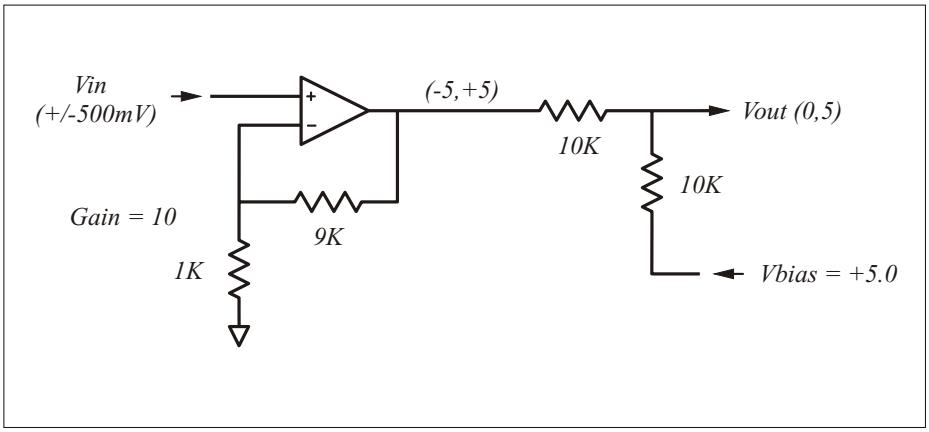

Figure 13: Op amp buffer with gain of 10

Generic bipolar op amps are often good choices for the amplifiers in these circuits. Parts such as the LM324 provide four amps at an exceptionally low price with good noise and other specs. Don't worry too much about op amp V_{io} input offset when using reasonable gains. In the above circuit, a LM324 with a typical 7mV V_{io} would result in 70mV of V_{out} offset. While you could use a higher grade amplifier, if the application is an interface to an A/D system the LM324 offset can often be removed as a calibration correction in software. Of course, temperature sensitive applications may require higher grade amps with less V_{io} TC.

One area of caution when using op amps, particularly as unity gain buffers, is in driving capacitive loads. Capacitive loading directly on the output of an op amp may cause the

amp to oscillate. For example, the capacitance of long cables can be enough to create trouble. Check your signals with an oscilloscope to make sure all is well. For those cases where driving a capacitive load is unavoidable, the circuit shown in Figure 14 is reasonable. If you are driving loads of varying capacitance, such as cables of varying lengths, you may wish to put a large cap on the output to swamp out the variations and make component values insensitive to the various loads. *Do not assume you will be lucky*: op amps with capacitive loads *will oscillate*. Typical values for DC and low frequency applications are shown in the circuit fragment. The design equations for Figure 14 go beyond the scope of this paper.

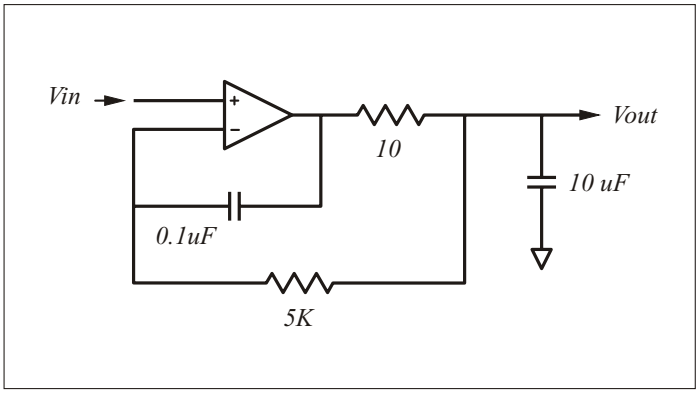

Figure 14: Op amp output circuit for capacitive loads

Besides using op amps to buffer passive resistor dividers as in the circuits above, it is also possible to bias signals by adjusting the operating point of the op amp itself. With this approach, the number of op amps required can sometimes be reduced. A popular circuit along these lines is the biased inverting amp:

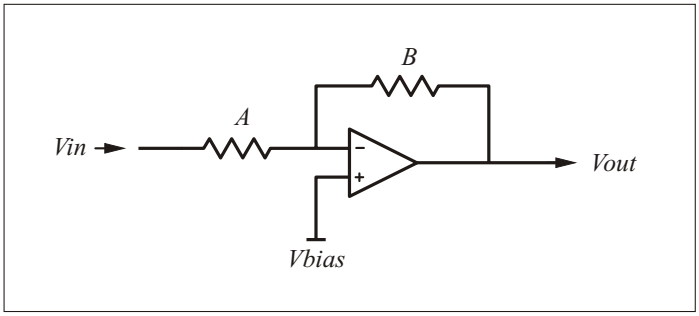

Figure 15: Biased inverting op amp circuit

The transfer function for this circuit is:

$$V_{out} \;=\; -\,(B/A)\cdot V_{in} \;+\; (1+B/A)\cdot V_{bias} \tag{25}$$

This equation is derived using the fact that the negative feedback drives the - input to match the + input, and the op amp input currents are negligible. As an example, if $A = 2B$ and $V_{bias} = 5/3$, then the transfer equation for Figure 15 is:

$$V_{out} \;=\; -\,V_{in}/2 \;+\; 2.5 \tag{26}$$

and an input range of (-5,+5) is mapped into an output range of (5,0). This result should be compared with equation (9) for a two resistor passive design, as well as comparing equations (25) and (6). The op amp circuit adds an inversion, but otherwise the design steps for various input and output ranges are comparable. As with a two resistor divider, odd bias voltages like 5/3 may be required. *However*, here you can generate the bias with a simple unbuffered resistor divider because the high input impedance of the op amp + input will not load the divider. Taking this approach Figure 15 becomes:

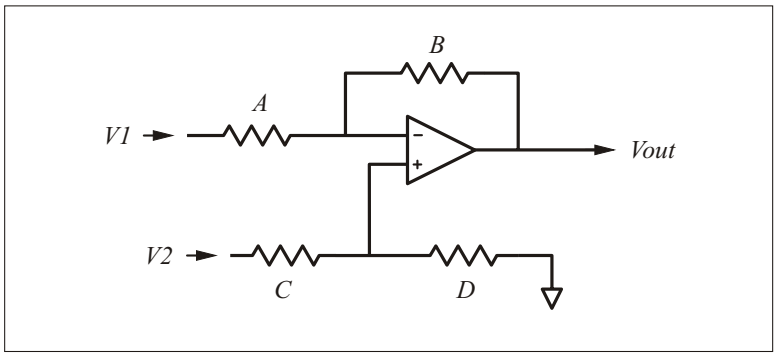

Figure 16: General difference op amp circuit

The transfer function for this is simply an extension to equation (25):

$$V_{out} \;=\; -\,(B/A)\cdot V_1 \;+\; (1+B/A)\cdot (D/(C+D))\cdot V_2 \tag{27}$$

where the inputs have been labeled V_1 and V_2 for generality. By selectively choosing (V_1, V_2) and (A, B, C, D) with this circuit, a surprising number of circuit variations are possible. A few special cases are given on the next page.

Special cases of equation (27) are:

Description : standard Inverting amplifier with bias, (Figure 15)
(V_1, V_2) (A, B, C, D) : $V_1 = V_{input}$, $V_2 = V_{bias}$, $C = 0$, $D = \infty$
Transfer function : $V_{out} = -(B/A) \cdot V_{input} + (1 + B/A) \cdot V_{bias}$

Description : standard Non Inverting amplifier with bias and gain >= 1
(V_1, V_2) (A, B, C, D) : $V_1 = V_{bias}$, $V_2 = V_{input}$, $C = 0$, $D = \infty$
Transfer function : $V_{out} = (1 + B/A) \cdot V_{input} + -(B/A) \cdot V_{bias}$

Description : Non Inverting amplifier with gain = 1/2
(V_1, V_2) (A, B, C, D) : $V_1 = V_2 = V_{input}$, $A = B$, $D = 3C$
Transfer function : $V_{out} = (1/2) \cdot V_{input}$

Description : standard Difference amplifier with unity gain
(V_1, V_2) (A, B, C, D) : $A = B = C = D$
Transfer function : $V_{out} = V_2 - V_1$

Despite the many special cases possible with Figure 16 and equation (27), the standard inverting amplifier with bias has several advantages. In particular, the following is often a good match for mapping (-5,+5) into (5,0) with $V_{bias} = +5$ volts:

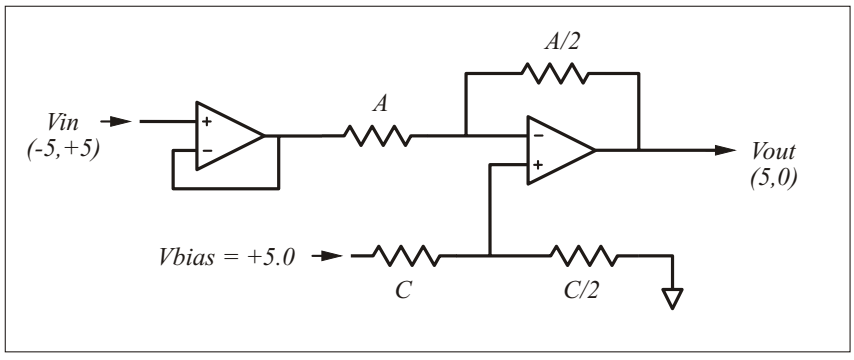

Figure 17: (-5,+5) to (5,0) inverting op amp circuit with bias

This circuit is particularly attractive because the inverting stage inputs are maintained

at a constant voltage by the negative feedback and do not see much common mode stress. Furthermore, with the inverting stage inputs at a constant voltage, *the bias source does not see any load variation with input signal*. This makes it much easier to maintain a precision constant bias. Finally, this configuration requires only a *positive* bias voltage.

By contrast, for a non-inverting circuit, the inputs would see full range common mode stress, a varying load would be placed on the bias source, and a negative bias would be required. Of course, a downside to the inverting amplifier is it does not have high input impedance. So a unity gain buffer has been added in Figure 17. This a reasonable tradeoff with many generic op amps optimized for unity gain performance. When constructing this circuit in the lab it is reasonable to make $A = C = 10K$ and build the $(A/2, C/2)$ resistors with pairs of 10K resistors in parallel. Depending on the op amp selection, it may even be possible to run the inverting stage from a single positive power supply.

Beyond op amps, instrument amps can also be used to perform scaling and biasing. This is usually done by applying the desired bias to the instrument amp reference pin. An instrument amp is typically several op amps on a single integrated circuit with a difference amp at its core. Instrument amps have good and bad points. A good point is they have matched resistor pairs as part of the integrated circuit substrate. This can be help improve common mode rejection for some differential applications. On the bad side, they are not as available as op amps, they do not have as wide a range of performance specs, they are more expensive, and they do not have standardized pin outs. The standardized pin outs of dual and quad op amps makes it easy to try a variety of parts with different specs in the same circuit. For instrument amp designs, manufacturer spec sheets should be consulted.

Summary

Several simple scaling and biasing techniques have been reviewed, along with the design equations for computing exact results. While other designs are certainly possible, the circuits presented here have proven simple and reliable for many applications. Among the most popular are:

- mapping (-5,+5) into (0,5) with a two resistor network
- mapping (-10,+10) into (0,5) with a three resistor network
- mapping (-5,+5) into (5,0) with a biased inverting op amp circuit

These circuits are capable of precision low noise performance with inexpensive components. If your input or output ranges differ from the specific examples given here, use the design steps or tables presented in the sections above to compute custom component values.

Parallel lines *never* meet
Caliente, Nevada, 2006

Scaling and Biasing Analog Signals

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